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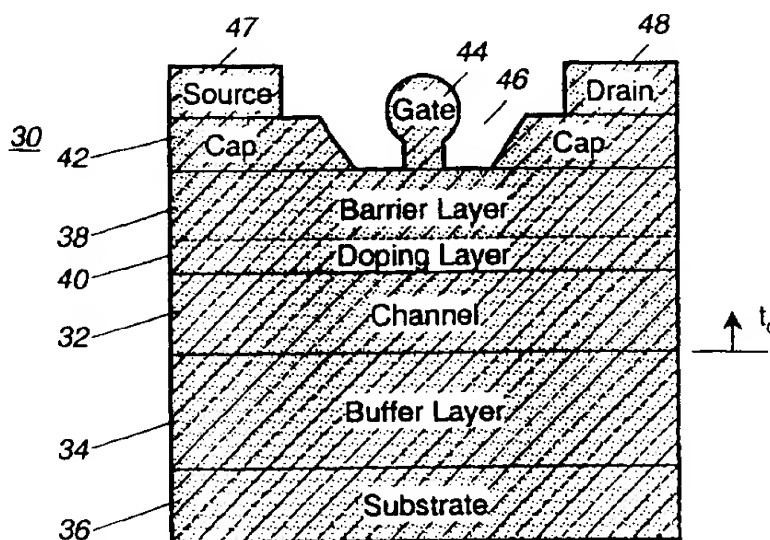
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(54) Partially relaxed channel HEMT device

(57) A HEMT device comprises a buffer layer disposed over a substrate. A partially-relaxed channel is disposed over the buffer layer and a barrier layer is dis-

posed over the channel. A cap layer is disposed over the barrier layer and a gate is positioned on the barrier layer. A source and a drain are positioned on the barrier layer on opposite sides of the gate.



Figur 2

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Description

BACKGROUND OF THE INVENTION

[0001] The present invention relates generally to High Electron Mobility Transistor (HEMT) devices and more particularly, to a HEMT device having a partially relaxed channel.

[0002] Referring to FIG. 1, a typical prior art HEMT device 10 comprises a buffer layer 12 which is grown on a substrate 14. A pseudomorphic channel 16 is grown on the buffer layer 12, and, a barrier layer 18 is grown on the channel 16. The barrier layer 18 typically includes a doping layer 20 disposed near the channel 16. A cap layer 22 is disposed on the barrier layer 18. The buffer layer 12 and the barrier layer 18 provide confinement of the carriers in the channel 16. The buffer layer 12 additionally isolates the channel 16 from the substrate 14. To complete the HEMT device 10, a gate 23 is positioned on the barrier layer 18 through a recess 24 formed in the cap layer 22. A source 24 and a drain 24 are positioned on the cap layer 22 on either side of the gate 23.

[0003] A thick channel 16 is desirable because a thicker channel 16 provides improved containment of the carriers which improves the electrical properties of the HEMT device 10. Therefore, it is desirable to fabricate the channel 16 as thick as possible. However, the thickness of the channel 16 is limited to a thickness which maintains the material in the channel 16 in a pseudomorphic state. In a pseudomorphic state, the material of the channel 16 is under strain with no defects in the material resulting from strain relaxation. Defects in the material of the channel 16 caused by strain relaxation begin to appear once the channel 16 is fabricated to a thickness greater than the critical thickness. When defects are present in the channel 16, the channel 16 is referred to as being either partially-relaxed or fully-relaxed. Partially-relaxed and fully-relaxed are terms used in the industry to distinguish between levels of defects in the material. A partially-relaxed material has some level of defects but not enough to cause the material to lose all beneficial material properties, whereas a fully-relaxed material has enough defects to cause the material to lose most of its beneficial properties.

[0004] Any level of defects in the material of the channel 16 are considered by those skilled in the art to be undesirable because defects are thought to reduce the DC and RF performance of the HEMT device 10. Therefore, the channel 16 of the prior art HEMT device 10 is only grown below the critical thickness, so that defects in the channel 16 can be avoided. This means that the typical HEMT device 10 has a relatively thin channel 16. A thin channel 16 poorly confines the carriers in the channel 16 which limits the gain and frequency response of the HEMT device 10.

[0005] What is desired therefore is a HEMT device which provides a higher gain and frequency response

than provided by the prior art HEMT device 10.

SUMMARY OF THE INVENTION

[0006] The proceeding and other shortcomings of the prior art are addressed and overcome by the present invention which provides a HEMT device comprising a buffer layer disposed on a substrate. A partially-relaxed channel is disposed on the buffer layer and a barrier layer is disposed on the channel. A cap layer is disposed on the barrier layer and a gate is positioned on the barrier layer. A source and a drain are positioned on the barrier layer on opposite sides of the gate.

[0007] In a second aspect the channel is fabricated of a material which, when disposed to a first thickness is pseudomorphic; and, when disposed to a second thickness, is fully-relaxed. The channel is fabricated to a thickness intermediate the first and second thicknesses.

[0008] In a third aspect, the present invention provides a method for fabricating a HEMT device having a gate, a source and a drain. A buffer layer is deposited on a substrate. A partially-relaxed channel is deposited on the channel and a barrier layer is deposited on the channel. A cap layer is deposited on the barrier layer and the gate is positioned on the cap layer through a recess formed in the cap layer. The source and the drain are positioned on the cap layer on opposite sides of the gate.

BRIEF DESCRIPTION OF THE DRAWINGS

[0009] Reference is now made to the detailed description of the preferred embodiments, illustrated in the accompanying drawings, in which:

FIG. 1 shows a cross-sectional view of prior art HEMT device;

FIG. 2 shows a cross-sectional view of a HEMT device in accordance with the preferred embodiment of the present invention; and,

FIG. 3 shows a graph comparing the frequency performance of HEMT devices having channel thicknesses of 15, 20 and 25 nm corresponding to partially relaxed channels with increasing defect densities, respectively.

DETAILED DESCRIPTION OF THE PREFERRED EMBODIMENTS

[0010] Referring to FIG. 2, the present invention addresses and overcomes the disadvantages of the prior art by providing a HEMT device 30 having a partially-relaxed channel 32 which is thicker than the pseudomorphic channel 16 (FIG. 1) of the prior art HEMT device 10. The partially-relaxed channel 32 (FIG. 2) does contain some defects which, as mentioned above, are considered by those skilled in the art to decrease the RF and DC performance of the HEMT device 30. However,

this has not proven to be the case. As will subsequently be discussed, tests have shown that a certain level of defects is acceptable and actually provides a HEMT device 30 having an improved RF and DC performance.

[0011] A HEMT device 30 in accordance with the present invention includes a buffer layer 34 disposed or grown over a substrate 36 and a channel 32 disposed or grown over the buffer layer 34. A barrier layer 38 is grown over the channel 32 and preferably includes a doping layer 40 near the channel 32. The doping layer 40 is preferably a Si planar doping layer. The buffer layer 34 and the barrier layer 38 provide confinement of the carriers in the channel 32. The buffer layer 34 additionally isolates the channel 32 from the substrate 14. To complete the HEMT device 30, a cap 42 is disposed on the barrier layer 38 and a gate 44 is positioned on the barrier layer 38 through a recess 46 formed in the cap layer 42. A source 47 and a drain 48 are positioned on the cap layer 42 on either side of the gate.

[0012] The buffer layer 34 and barrier layer 38 both provide containment of the carriers in the channel 32. To do so, the buffer layer 34 and barrier layer 38 must each be fabricated of a different material than the channel 32. In addition, the lattice constant of the material comprising the channel 32 must be different than the lattice constant of each of the materials comprising the buffer layer 34 and the barrier layer 38. A strain exists between the buffer layer 34 and the channel 32 because the lattice constant of the channel 32 is different than the lattice constant of the buffer layer 34. The strain increases as the channel thickness t_c is increased. The material of the channel 32 can tolerate a certain level of strain without generating defects in the material of the channel 32. As such, the channel 32 can be fabricated to a predetermined thickness t_c free of defects. The defect-free state is known as a pseudomorphic state. At a certain higher level of strain associated with a thicker channel 32, defects appear in the material of the channel 32. This defect-containing state is known as a partially-relaxed state. When the channel 32 is fabricated even thicker, the strain further increases and the number of defects in the material of the channel 32 increases until a sufficient number of defects exist in the material of the channel 32 to reduce virtually all the desirable properties of the material. This state is known as a fully-relaxed state.

[0013] The exact thickness t_c at which the channel 32 becomes partially-relaxed or fully relaxed is determined by the material properties of the channel 32 as well as the material properties of the buffer layer 34. For example, in an InP based HEMT device having an InAlAs buffer layer 34 and an InGaAs channel 32 with 75% In, the channel 32 is pseudomorphic below a thickness of approximately 15 nanometers and is fully-relaxed above a thickness of about 30 nanometers. The channel 32 is thus partially-relaxed between a thickness of about 15 and 30 nanometers. In contrast, for a GaAs based HEMT device having a composite GaAs/AlGaAs buffer

layer 34 and an InGaAs channel 32 with 21% In, the channel 32 is pseudomorphic below a thickness of approximately 15 nanometers and is fully-relaxed above a thickness of about 22 nanometers. The channel 32 is partially-relaxed between a thickness of about 15 and 22 nanometers.

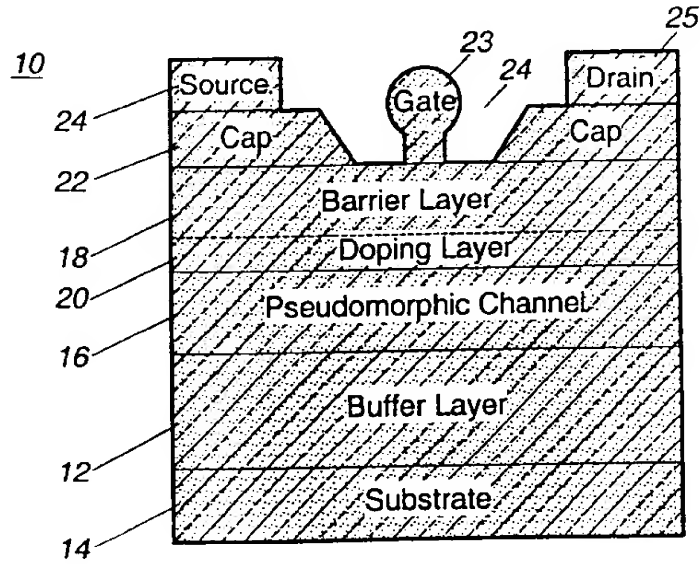
[0014] Referring to FIGs. 2 & 3, HEMT devices 30 having 15, 20 and 25 nm thick channels 32 were fabricated and tested. Thicknesses of 15, 20 and 25 nm correspond to pseudomorphic, partially-relaxed and fully-relaxed channels 32 respectively. For each of these HEMT devices, the buffer layer 32 was fabricated of an InAlAs material to a thickness of 300 nm; the channel 32 was fabricated of an InGaAs material which comprised 75% In; and, the barrier layer 38 was fabricated of 280 nm thick InAlAs material which included a Si planar doping layer 40 near the channel 32. The cap 42 was fabricated of an InGaAs material. The frequency response (FT) of each HEMT device was measured and is shown graphically in FIG. 3. As depicted in this graph, the HEMT device having a partially-relaxed channel (channel thickness = 20 nm) provided an improved frequency response when compared to a HEMT device having a pseudomorphic channel (channel thickness = 15 nm) or a HEMT device having a partially relaxed channel (channel thickness = 25 nm) with a higher degree of relaxation.

[0015] As will be appreciated by one skilled in the art, the present invention is not limited to the structures and figures shown and described hereinabove but can be practiced with any HEMT device known to one skilled in the art in which the lattice constant of the channel is different than the lattice constant of the buffer layer. For example, the present invention can be practiced in an AlGaIn/GaN/InGaIn HEMT device or an AlGaInSb/InSb/GaSb HEMT device. It will be appreciated that many variations of the invention are possible and the invention is limited only by the claims which follow.

Claims

1. A high electron mobility transistor (HEMT) device comprising:
 - a buffer layer disposed over a substrate;
 - a partially-relaxed channel disposed over said buffer layer;
 - a barrier layer disposed over said channel;
 - a cap layer disposed over said barrier layer;
 - a gate positioned on said barrier layer; and
 - a source and a drain positioned on said cap layer.

2. A HEMT device as in claim 1, further comprising a doping layer disposed on said channel.
3. A HEMT device as in claim 1, wherein said channel is fabricated of a material which when disposed to a first thickness is pseudomorphic and when disposed to a second thickness is fully relaxed, said channel having a thickness intermediate said first and second thicknesses.
4. A HEMT device as in claim 3, wherein said channel comprises an InGaAs material.
5. A HEMT device as in claim 1, wherein said partially relaxed channel comprises a material having a lattice constant, said buffer layer comprising a material having a lattice constant different than the lattice constant of the channel material.
6. A method for fabricating a HEMT device having a gate, a source and a drain comprising the steps of:
 - depositing a buffer layer over a substrate;
 - depositing a partially-relaxed channel over said buffer layer;
 - depositing a barrier layer over said channel;
 - depositing a cap layer over said barrier layer;
 - positioning the gate on the barrier layer; and
 - positioning the source and the drain at preselected locations on the cap layer.
7. The method of claim 6, wherein depositing a channel material comprises depositing a channel material comprising InGaAs material over said buffer layer to a thickness which results in said channel being in a partially relaxed state; and, wherein depositing a buffer layer comprises depositing a buffer layer over an InP-based substrate.
8. The method of claim 6, wherein depositing a channel material comprises depositing a composite GaAs/InGaAs material over said buffer layer to a thickness which results in said channel being in a partially relaxed state; and, wherein depositing a buffer layer comprises depositing a buffer layer over an InP-based substrate.
9. The method of claim 6, wherein depositing a channel material comprises depositing a composite GaAs/InGaAs material over said buffer layer to a thickness which results in said channel being in a partially relaxed state.
10. The method of claim 6, wherein positioning the gate on the barrier layer comprises forming a recess in the cap layer to expose a portion of the barrier layer; and positioning the gate on the exposed portion of the barrier layer.
11. The method of claim 6, further comprising depositing a doping layer on said channel layer.



Prior Art
Figure 1

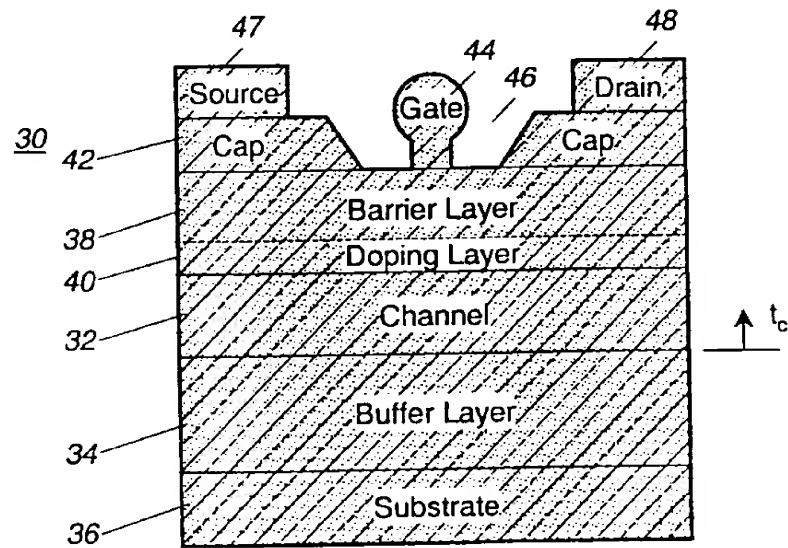


Figure 2

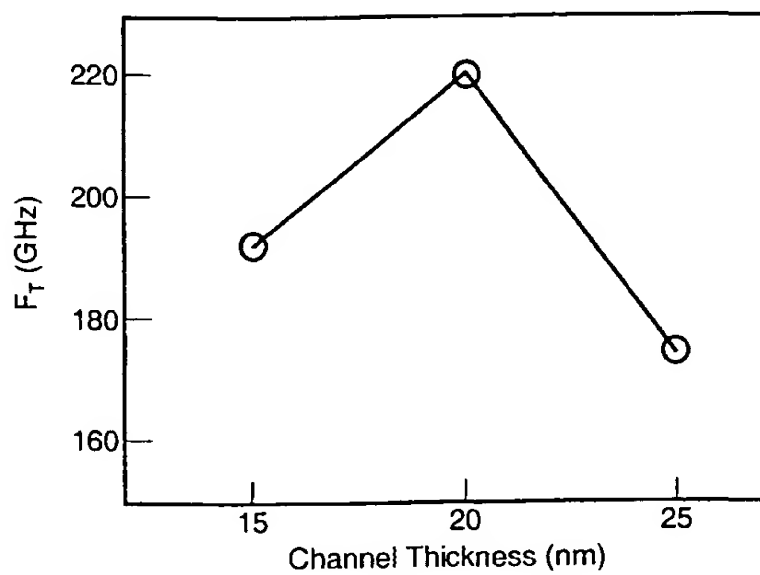


Figure 3